

REMARKS

Examiner J. Trimmings is thanked for the thorough examination and search of the subject Patent Application. Claims 1, 8, and 13 have been amended. Claims 7 and 19 have been canceled.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 1, 8, and 13 rejected under 35 USC 112, second paragraph as being indefinite is requested based on Amended Claims 1, 8, and 13, and on the following remarks.

Claims 1, 8, and 13 have been amended to remove the indefiniteness cited by the Examiner. In particular, Amended Claim 1 now reads:

1. (Currently Amended) A method to verify the performance of a built-in self-test circuit for testing embedded memory in an integrated circuit device comprising:

introducing a set of faults into an embedded memory  
5 behavior model wherein said embedded memory behavior model comprises a high-level language model and wherein each

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member of said set of faults comprises a finite state  
machine state, a memory address, and a memory data fault;  
thereafter simulating said built-in self-test circuit  
10 and said embedded memory behavior model wherein said built-  
in self-test circuit generates input data and address  
patterns for said embedded memory behavior model, wherein  
said embedded memory behavior model outputs memory address  
and data in response to said input data and address  
15 patterns, and wherein said input address and data and said  
memory address and data are compared in said built-in self-  
test circuit and a fault output is generated if not  
matching;  
de-scrambling said set of faults; and  
20 comparing said fault output and said de-scrambled set  
of faults to verify the performance of said built-in self-  
test circuit.

As shown above, Claim 1 has been amended such that the reference  
to "set of faults" in line 20 clearly designates the "de-  
scrambled" set of faults of line 19. This amendment should make  
Claim 1 definite with respect to 35 USC 112, second paragraph.

Similarly, Claim 8 has been amended as shown below:

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8. (Currently Amended) A method to verify the performance of a built-in self-test circuit for testing embedded memory in an integrated circuit device comprising:

introducing a set of faults into an embedded memory  
5 behavior model wherein said embedded memory behavior model comprises a high-level language model and wherein each member of said set of faults comprises a finite state machine state, a memory address, and a memory data fault;  
thereafter simulating said built-in self-test circuit  
10 and said embedded memory behavior model wherein said built-in self-test circuit generates input data and address patterns for said embedded memory behavior model, wherein said input data and address patterns are scrambled prior to input into said embedded memory behavior model, wherein  
15 said embedded memory behavior model outputs memory address and data in response to said input data and address patterns, and wherein said memory address and data are de-scrambled and then are compared to said input address and data in said built-in self-test circuit and a fault  
20 output is generated if not matching;  
de-scrambling said set of faults; and  
thereafter comparing said fault output and said de-scrambled set of faults to verify the performance of said built-in self-test circuit.

In this case, line 23 has been amended such that the "de-scrambled" set of faults is referenced in line 23. This amendment should make Claim 8 definite with respect to 35 USC 112, second paragraph.

Similarly, Claim 13 has been amended as shown below:

13. (Currently Amended) An apparatus to verify the performance of a built-in self test circuit for testing embedded memory in an integrated circuit device comprising:

an embedded memory behavior model wherein said  
5 embedded memory behavior model comprises a high-level language model;

a built-in self-test circuit model connected to said embedded memory behavior model wherein said built-in self-test circuit model generates input data and address  
10 patterns for said embedded memory behavior model, wherein said embedded memory behavior model outputs memory address and data in response to said input data and address patterns, and wherein said memory address and data are compared to said input address and data in said built-in  
15 self-test circuit and a fault output is generated if not matching;

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a means of introducing a set of faults into said  
embedded memory behavior model wherein each member of said  
set of faults comprises a finite state machine state, a  
20 memory address, and a memory data fault;  
a means of simulating said embedded memory behavior  
model and said built-in self-test circuit model;  
a means of de-scrambling said set of faults; and  
a means of comparing the fault ~~diagnosis~~ output  
25 of said built-in self-test circuit model and said  
de-scrambled set of faults to verify the performance of  
said built-in self-test circuit.

In this case, line 26 has been amended such that the "de-scrambled" set of faults is referenced in line 26. Further, the word "diagnosis" in line 24 is removed due to lack of antecedent basis. This amendment should make Claim 13 definite with respect to 35 USC 112, second paragraph.

Reconsideration of Claims 1, 8, and 13 rejected under 35 USC 112, second paragraph as being indefinite is requested based on Amended Claims 1, 8, and 13, and on the following remarks.

Reconsideration of Claims 1-4, 6, 8-11, 13-16, and 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Bo Lu

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(U.S. 6,012,157), and in view of Takahashi Ohsawa (U.S. 5,748,641) is requested based on Amended Claims 1, 8, and 13, and on the following remarks.

As stated by the Examiner in the present action, the Examiner and the Applicant agree that the subject matter of Lu does not teach the de-scrambling of the set of faults. Further, Applicant's claimed invention, as recited in Amended Claims 1, 8, and 13, now clearly and definitively teaches this feature of de-scrambling of the set of faults. Therefore, Applicant believes that Amended Claims 1, 8, and 13 are definite and distinct with respect to the cited art and, further, that the cited art does not teach nor suggest Applicant's Claimed invention including the feature of de-scrambling the set of faults. Therefore, Applicant respectfully requests that the rejection of Claims 1, 8, and 13 under 35 USC 103(a) be removed in light of the above-described amendments. Finally, Claim 2-6, 9-11, 14-16, and 20 represent patentably distinct, further limitations on Claims 1, 8, and 13, and therefore should not be rejected under 35 USC 103(a) if Claims 1, 8, and 13 are not rejected.

Reconsideration of Claims 1-4, 6, 8-11, 13-16, and 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Bo Lu

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(U.S. 6,012,157), and in view of Takahashi Ohsawa (U.S. 5,748,641) is requested based on Amended Claims 1, 8, and 13, and on the above remarks.

Reconsideration of Claims 5, 12, 17, and 20 rejected under 35 U.S.C. 102(b) as being unpatentable over Bo Lu (U.S. 6,012,157), and in view of Takahashi Ohsawa (U.S. 5,748,641) as applied to Claims 1, 8, and 13, above, and further in view of SynTest Technologies, Inc., March 1999, is requested based on Amended Claims 1, 8, and 13, and on the following remarks.

As discussed above, Amended Claims 1, 8, and 13 should now contain patentable subject matter over the cited art of Bo Lu. Further, Amended Claims 1, 8, and 13 now contain a key feature not taught or suggested by Bo Lu and describe that key feature in a definitive way. Further yet, the cited art of Bo Lu, Takahashi Ohsawa, and SynTest Technologies, Inc. do not, separately or taken together, teach or suggest, the key feature of de-scrambling the set of faults as recited in Applicant's invention. Therefore, Applicant respectfully requests that the rejection of Claims 1, 8, and 13 under 35 USC 103(a) be removed in light of the above-described amendments. Finally, Claim 2-6, 5, 12, 17, and 20 represent patentably distinct, further limitations on Claims 1, 8, and 13, and therefore should not be

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rejected under 35 USC 103(a) if Claims 1, 8, and 13 are not rejected.

Reconsideration of Claims 5, 12, 17, and 20 rejected under 35 U.S.C. 102(b) as being unpatentable over Bo Lu (U.S. 6,012,157), and in view of Takahashi Ohsawa (U.S. 5,748,641) as applied to Claims 1, 8, and 13, above, and further in view of SynTest Technologies, Inc., March 1999, is requested based on Amended Claims 1, 8, and 13, and on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and have discussed their impact on the present invention above.

Allowance of all Claims is requested.

It is requested that should the Examiner not find that the Claims are now Allowable that the Examiner call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'SBA', is written over the printed name of Stephen B. Ackerman.

Stephen B. Ackerman, Reg. No. 37,761